UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,878,576 B1
APPLICATION NO. : 10/716991
DATED : April 12, 2005
INVENTOR(S) : Mears et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

The title page showing the print figure should be deleted, and replaced with the attached amended title page.

On the title page, Item (56), References Cited,
Insert: "H01L 29/14" after "EP 0393135 11/1994"

In the Drawings

Delete: FIG. 1
Insert: New FIG. 1

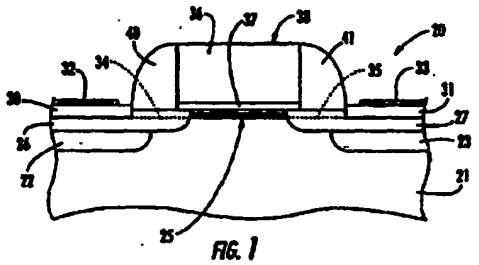

FIG. 1

Delete: FIG. 2
Insert: New FIG. 2

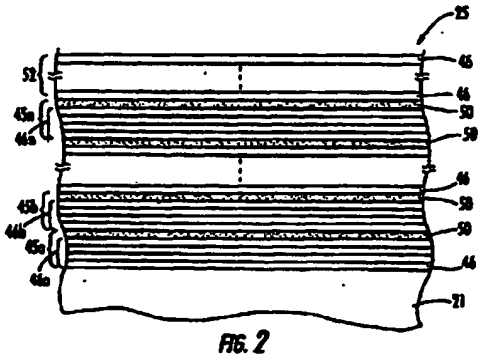

FIG. 2

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In the Drawings	Delete: FIG. 4 Insert: New FIG. 4

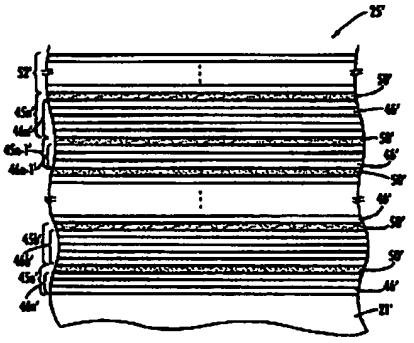

FIG. 4

Column 1, Line 67	Delete: "in a silicon" Insert: --in silicon--
Column 2, Line 1	Delete: "electromuminescence" Insert: --electroluminescene--
Column 2, Line 60	Delete: "superlattice and has" Insert: --superlattice has--
Column 5, Line 14	Delete: "gate 35" Insert: --gate 38--
Column 5, Line 62	Delete: "gate 35" Insert: --gate 38--
Column 7, Line 66	Delete: "from the both" Insert: --from both--
Column 9, Lines of 46-48	Delete: "In other processes and devices the structures the present invention may be formed on a portin of a wafer or across substantially all of a wafer."

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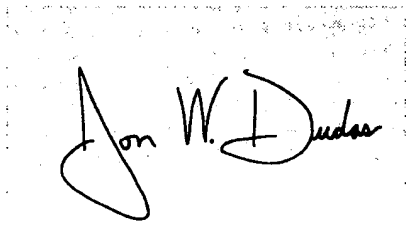
Column 9, Line 61	Delete: "also formed" Insert: --also be formed--

Signed and Sealed this

Thirty-first Day of October, 2006



JON W. DUDAS
Director of the United States Patent and Trademark Office

(12) **United States Patent**
Mears et al.

(10) **Patent No.: US 6,878,576 B1**
(45) **Date of Patent: Apr. 12, 2005**

(54) **METHOD FOR MAKING SEMICONDUCTOR DEVICE INCLUDING BAND-ENGINEERED SUPERLATTICE**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/716,991**

(22) Filed: **Nov. 19, 2003**

Related U.S. Application Data

(63) Continuation of application No. 10/647,061, filed on Aug. 22, 2003, which is a continuation-in-part of application No. 10/603,696, filed on Jun. 26, 2003, and a continuation-in-part of application No. 10/603,621, filed on Jun. 26, 2003.

(51) **Int. Cl.**[7] **H01L 21/20**
(52) **U.S. Cl.** **438/162**; 438/479; 438/301
(58) **Field of Search** 438/22–47, 149–162, 438/217, 222–228, 229–301, 479–508

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(57) **ABSTRACT**

A method is for making a semiconductor device by forming a superlattice that, in turn, includes a plurality of stacked groups of layers. The method may also include forming regions for causing transport of charge carriers through the superlattice in a parallel direction relative to the stacked groups of layers. Each group of the superlattice may include a plurality of stacked base semiconductor monolayers defining a base semiconductor portion and an energy band-modifying layer thereon. The energy-band modifying layer may include at least one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions so that the superlattice may have a higher charge carrier mobility in the parallel direction than would otherwise occur. The superlattice may also have a common energy band structure therein.

36 Claims, 9 Drawing Sheets